A MANUFACTURABLE GaAs MMIC AMPLIFIER WITH 10 GHz BANDWIDTH

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ABSTRACT

A two stage feedback amplifier has been developed for the 2 to 12 GHz band. The measured gain is 10 ± 1 dB with 2.5:1 input and 1.7:1 output VSWR. The chip size is less than 0.5 x 1.0 mm^2 and it includes complete RF and bias circuitry. The amplifier also has AGC capability with more than 25 dB of gain control.

INTRODUCTION

Wideband microwave amplifiers are important building blocks for modern electronic countermeasures and surveillance systems. Feedback amplifiers have shown good tolerance to device variations as well as wide bandwidth.[1,2,3] To implement a feedback amplifier design with more than 10 dB gain over a 10 Ghz bandwidth, two or more amplifier stages are generally required. Additionally, for an MMIC amplifier to be manufacturable, it is important to keep the chip size small. This paper describes a two-stage feedback amplifier in which a high degree of chip miniaturization is achieved by using a novel, direct coupling scheme. The direct coupling of the two stages eliminates the need for an interstage blocking capacitor and the associated extra bias circuitry. The complete matched amplifier is realized in a 0.5 x 1 mm^2 area resulting in more than 3500 potential MMIC chips on a 2" diameter wafer. A gain of 10 ± 1 dB is measured between 2 and 12 GHz. The small size of the amplifier chip also allows packaging in conventional microwave transistor packages.

CIRCUIT DESIGN

A two-stage resistive feedback design is employed to provide the required gain and VSWR over the 10 GHz bandwidth. A single power supply is sufficent to provide all the required potentials for chip operation. Bias is applied to the drain terminal of the second stage FET. The same power supply biases the first stage FET directly through the second stage feedback resistor. Figure 1 shows the schematic of the complete two -stage amplifier.

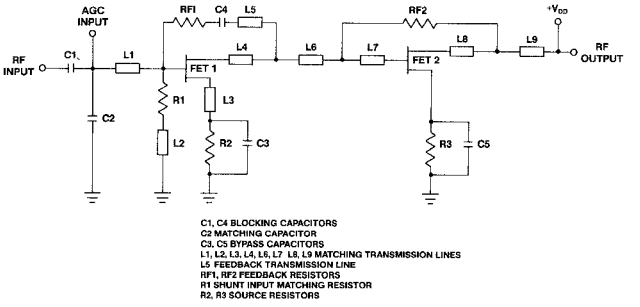

Figure 1
Schematic of the Single-Power-Supply Two-Stage Amplifier

The DC operating point of the first FET is determined by the source resistor R2 and the feedback resistor RF2. The first FET is biased at a low drain current level to achieve a lower amplifier noise figure. The DC operating point of the second FET is determined by the drain voltage of the first FET (which is directly connected to the gate of the second FET) and by the source resistor R3. The second stage is biased at a higher drain current level to provide higher gain and power. In this design +8V and 55 mA are typical DC amplifier supply conditions.

The choice of the gate width and length of the FETs is based on an optimization among several requirements: gain, gain flatness,

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and VSWR. FETs with gate dimensions of 500 µm x 0.5 µm are used for both stages. Some reactive interstage matching is used to improve the gain flatness. Low output VSWR can be easily obtained as the output impedance of the FET is near the center of the Smith chart in the frequency band of interest. It is more difficult to achieve low input VSWR over the 10 GHz bandwidth. To achieve the required input VSWR, a shunt L-R network combined with a low-pass reactive matching network is added at the input. An in-house computer analysis and optimization program (AMCAP) was used extensively in the design. Figure 2 is the computer simulated results of the gain and VSWR of the MMIC amplifier. The gain at 2 GHz is limited mainly by the size of the source bypass capacitors (C3 and C5, being about 6 PF each). A larger source capacitance value (which means larger GaAs chip area) raises the gain at 2 Ghz to that at the middle of the band.

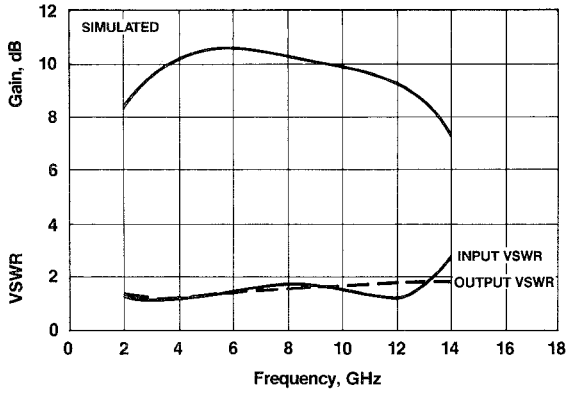

Figure 2
Simulated Gain and VSWR of the Amplifier

Higher gain amplifier blocks are realized by directly cascading the chips. An input blocking capacitor is included on the chip for this purpose. AGC operation is also available on this amplifier. By applying a negative voltage to the input of the amplifier, 25 dB of gain control is obtained.

FABRICATION

The IC process is an extension of a highly uniform GaAs FET process. The transistors are fabricated with a plated gate process which minimizes the gate resistance and improves the device reliability.[4] The gate employs a Ti/W/Au refractory metallization system. GaAs resistors are realized with the same active layer as is used for the transistors. Resistors in the range of 30 Ω to 10,000 Ω are fabricated easily. Capacitors are realized with metal-insulator-metal structures using Si_3N_4 as the insulator layer. The RF and DC grounding is achieved using a wraparound ground technique.[1] A photograph of the fabricated MMIC chip is shown in Figure 3.

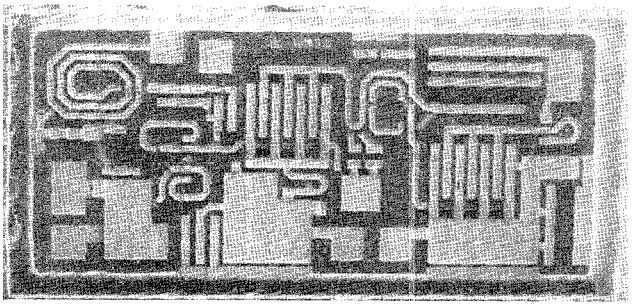

Figure 3
SEM Photograph of the Amplifier Chip

MEASURED RESULTS

Functional dice are selected by extensive automated DC wafer probing followed by visual inspection. Defective dice are identified by measuring the drain current, transconductance, and pinch-off voltage of the individual transistors as well as the values of the resistors (except the resistor RF1). The DC functional die is then mounted on a metallized alumina test carrier, which is via-hole grounded at the center and has 50 Ω input and output microstrip lines on each side. When the power-supply is applied, a properly biased amplifier will exhibit the DC I-V characteristic shown in Figure 4.

The DC supply current increases from zero at a rate of about 10 mA/V until the DC voltage supply approaches +2.0V. Above 2.0V, the DC current increases at about 5 mA/V due to the initiation of self-biasing of the second FET. This two section I-V curve is the characteristic signature of a properly biased amplifier.

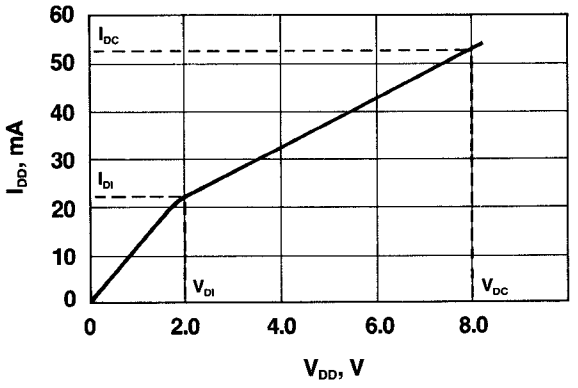

Figure 4
DC Characteristics of the Amplifier

Figure 5 is the measured RF performance of the gain and VSWR of the amplifier. In good agreement with the simulated results, the measurements show 10 ± 1 dB gain across the 2-12 GHz band. The input VSWR reaches a 2.5:1 maximum across the band. This is slightly higher than the design goal of 2:1. The discrepancy between the input VSWR measurements and simulations is attributed to incorrect transmission line lengths used for the input matching circuit inductors. It is found that the effective transmission line lengths of these spiral inductors should be reduced compared to their physical lengths owing to the tight coupling between adjacent lines of the inductor. The input VSWR is expected to meet the design goal with the next design iteration. The output VSWR is better than 1.7:1 across the band. The noise figure is measured to be typically 6 dB with a maximum noise figure of 8 dB being measured at 2 GHz. This noise figue result is also consistent with the simulated performance.

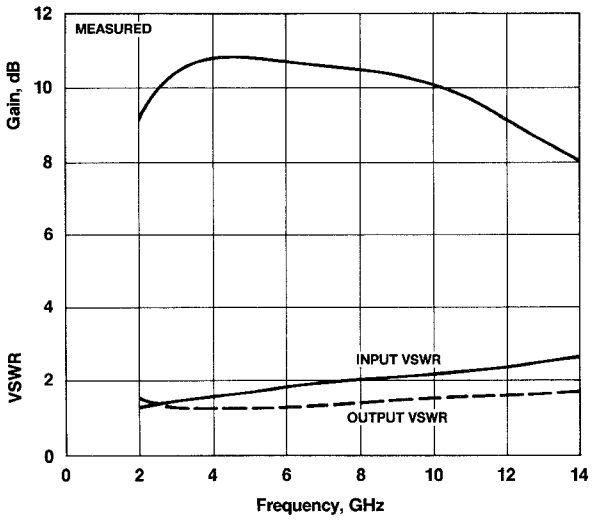

Figure 5
Measured Gain and VSWR of the Amplifier

The output power versus input power of the chip amplifier is shown in Figure 6. At the nominal bias voltage of +8V, a saturated power output of about +13 dBm is obtained across the band. With a higher bias voltage of +12V, a saturated power output of +15 dBm is obtained.

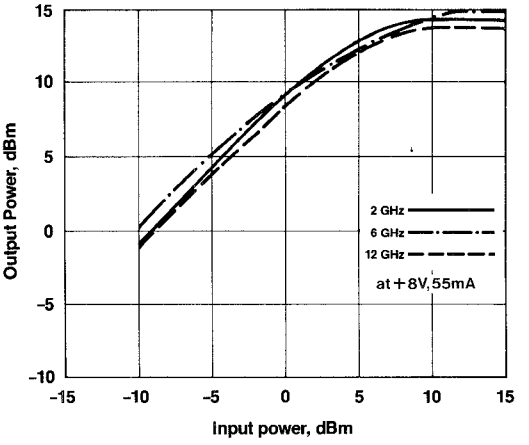

Figure 6
P_{OUT} VS. P_{IN} of the Amplifier

Another feature of this MMIC amplifier is that it can be used as an AGC amplifier. By applying a negative DC voltage to the amplifier input (which is also the gate of the first FET), the gain of the amplifier reduces due to the reduction in transconductance of the first FET.

Figure 7 shows the AGC performance of the amplifier. A gain variation of more than 25 dB across the 10 GHz bandwidth is realized without degrading the input VSWR. Gain flatness over most of the AGC control range is also maintained.

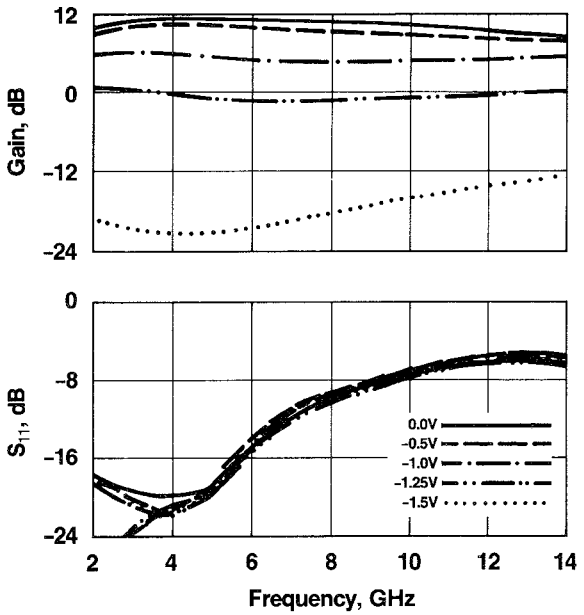

Figure 7
AGC Response of the Amplifier to a Negative DC Voltage Applied to the DC Input of the Amplifier

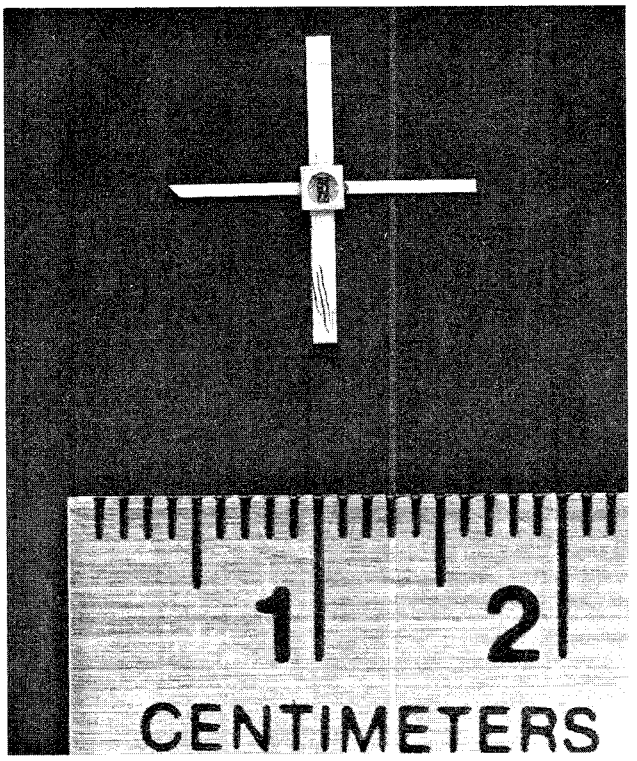

Figure 8
Photograph of the Two-Stage MMIC Amplifier in a 70 mil Stripline Package

Since the size of the MMIC chip is less than 0.5 x 1.0 mm^2, it can fit easily into a variety of microwave device packages. An example of such a packaged amplifier is shown in Figure 8 where the chip amplifier is assembled in 70 mil stripline package. Measured performance of this packaged amplifier showed satisfactory gain and VSWR up to 12 GHz.

SUMMARY

Design and performance of a two-stage, resistive feedback, direct-coupled amplifier is described. This amplifier provides 10 ± 1 dB gain across the 2 to 12 GHz band. The size of this MMIC amplifier chip is reduced to below 0.5 x 1.0 mm^2 by utilizing a novel bias scheme. The resulting large number of die per wafer makes this chip amplifier attractive for manufacturing. The chip amplifier also provides AGC operation and allows multi-stage cascading and conventional microwave transistor packaging.

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